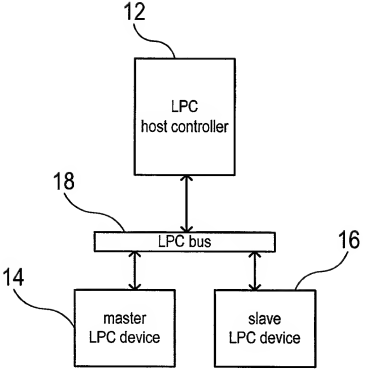

FIG. 1
(PRIOR ART)

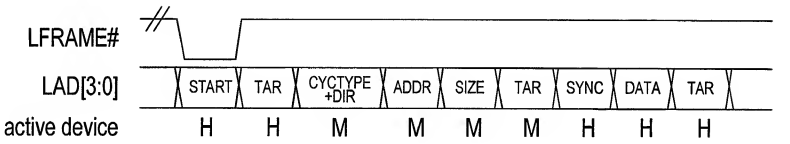

FIG. 2A （PRIOR ART）

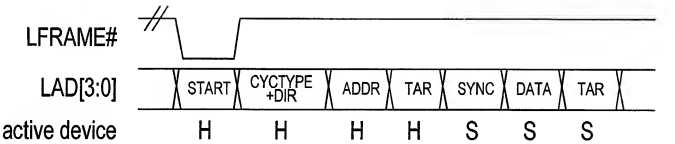

FIG. 2B （PRIOR ART）

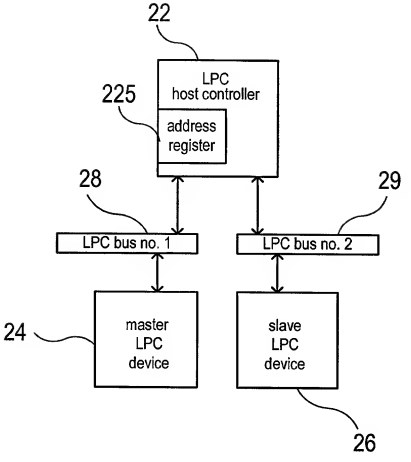
22
LPC
host controller
225
address
register
28
29
LPC bus no. 1
LPC bus no. 2
24
master
LPC
device
slave
LPC
device
26

FIG. 3

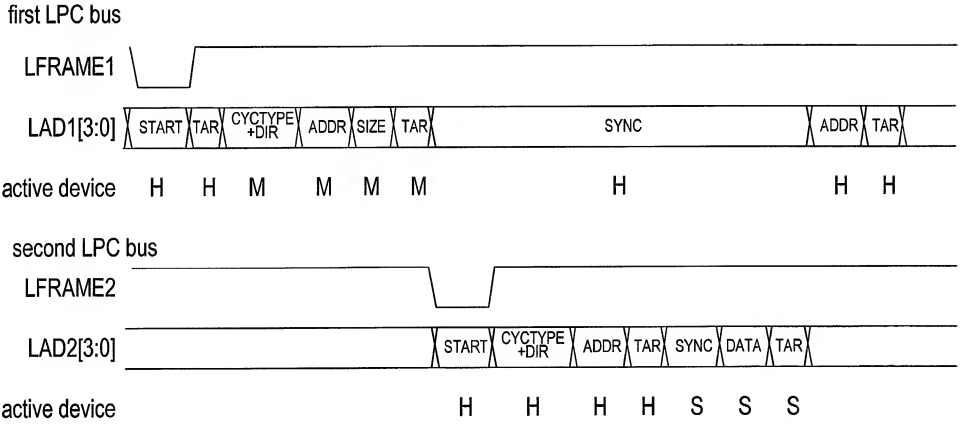

FIG. 4

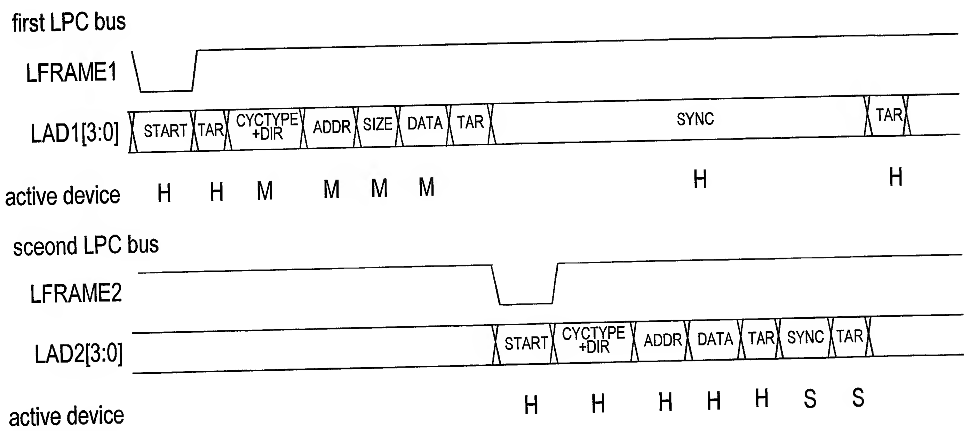
first LPC bus
LFRAME1
LAD1[3:0]
START
TAR
CYCTYPE +DIR
ADDR
SIZE
DATA
TAR
SYNC
TAR
active device
H H M M M M H H
sceond LPC bus
LFRAME2
LAD2[3:0]
START
CYCTYPE +DIR
ADDR
DATA
TAR
SYNC
TAR
active device
H H H H H S S

FIG. 5

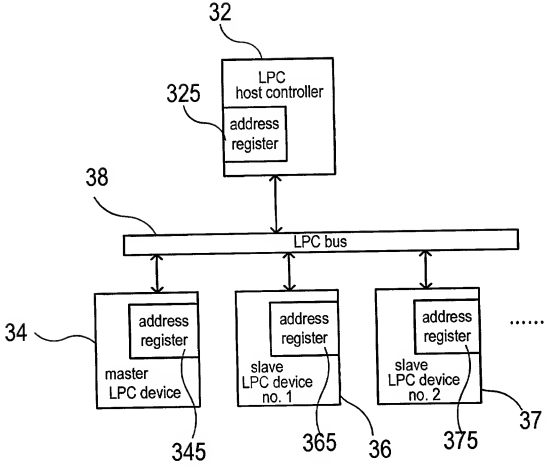
32
LPC
host controller
325
address
register
38
LPC bus
34
address
register
master
LPC device
345
address
register
slave
LPC device
no. 1
365
36
address
register
slave
LPC device
no. 2
375
37
.....

FIG. 6

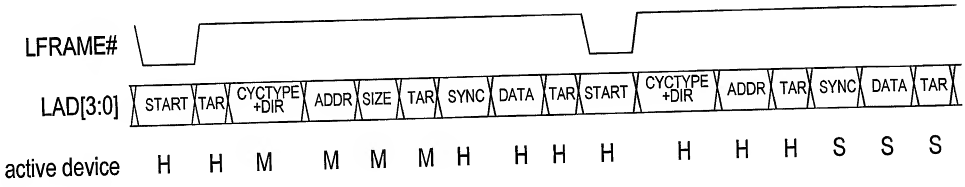
LFRAME#
LAD[3:0]
START
TAR
CYCTYPE +DIR
ADDR
SIZE
TAR
SYNC
DATA
TAR
START
CYCTYPE +DIR
ADDR
TAR
SYNC
DATA
TAR
active device
H H M M M M H H H H H H H S S S

FIG. 7

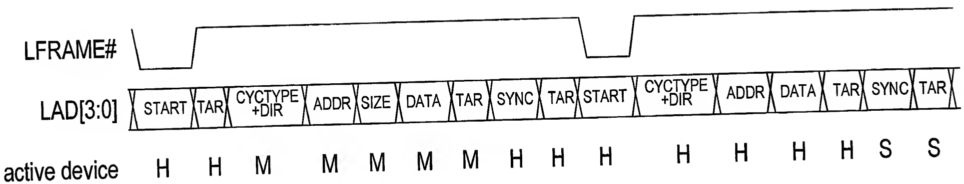
LFRAME#
LAD[3:0]
START
TAR
CYCTYPE +DIR
ADDR
SIZE
DATA
TAR
SYNC
TAR
START
CYCTYPE +DIR
ADDR
DATA
TAR
SYNC
TAR
active device
H H M M M M M H H H H H H H S S

FIG. 8